IN THE CLAIMS

1. (Original) A method comprising:

detecting a bus arbitration event between at least a first bus agent and a second bus agent; and

granting concurrent bus ownership to the first bus agent and the second bus agent if the first bus agent and the second bus agent have different grant-to-valid latencies.

2. (Original) The method of claim 1, wherein detecting the bus arbitration event comprises:

detecting assertion of at least a first bus request signal and a second bus request signal during a single clock cycle.

3. (Original) The method of claim 1, wherein prior to granting concurrent bus ownership, the method further comprises:

determining a grant-to-valid latency of the first bus agent as a first grant-to-valid latency;

determining a grant-to-valid latency of the second bus agent as a second grant-to-valid latency; and

comparing the first grant-to-valid latency to the second grant-to-valid latency to determine whether the first grant-to-valid latency is equal to the second grant-to-valid latency.

4. (Original) The method of claim 2, wherein the first bus request signal and the second bus request signal are one of an address bus request signal and a data bus request signal.

5. (Original) The method of claim 1, wherein granting concurrent bus ownership comprises:

asserting a bus grant signal to both the first bus agent and the second bus agent in a next clock cycle.

6. (Original) The method of claim 1, further comprising:

selecting one of the first bus agent and the second bus agent as a selected bus agent according to a predetermined arbitration standard if a grant-to-valid latency of the first bus agent is equal to a grant-to-valid latency of the second bus agent; and

granting bus ownership to the selected bus agent.

7. (Original) The method of claim 1, wherein the predetermined arbitration standard is a round-robin arbitration scheme.

8. (Currently Amended) The method of claim 1, further comprising:

deasserting a bus grant signal to one of the first bus agent and the second bus agent having a lower grant-to-valid latency in clock cycle n, where n is an integer greater than one (1); and

deasserting a bus grant signal to one of the first bus agent and the second bus agent having a greater grant-to-valid latency in clock cycle n+1.

9. (Original) The method of claim 5, wherein the bus grant signal is one of an address bus grant signal and a data bus grant signal.

10. (Original) The method of claim 1, wherein the first bus agent and the second bus agent are symmetric bus agents.

11. A bus arbiter comprising:

a controller to detect a bus arbitration event between at least a first bus agent and a second bus agent, the controller to grant concurrent bus ownership to the first bus agent and a second bus agent if the first bus agent and the second bus agent have unequal grant-to-valid latencies.

12. (Original) The bus arbiter of claim 11, wherein the controller comprises:

arbitration logic to determine a grant-to-valid latency of the first bus agent as a first grant-to-valid latency, to determine a grant-to-valid latency of the second bus agent as a second grant-

to-valid latency and to compare the first grant-to-valid latency to the second grant-to-valid latency to determine whether the first grant-to-valid latency is equal to the second grant-to-valid latency.

13. (Original) The bus arbiter of claim 11, wherein the controller comprises:

arbitration logic to detect assertion of at least a first bus request signal and a second bus request signal during a single clock cycle.

14. (Original) The bus arbiter of claim 11, wherein the first bus request signal and the second bus request signal are one of an address bus request signal and a data bus request signal.

15. (Original) The bus arbiter of claim 11, wherein the controller comprises:

assertion logic to assert a bus grant signal to both the first bus agent and the second bus agent in a next clock cycle.

16. (Currently Amended) The bus arbiter of claim 11, wherein the controller comprises:

assertion logic to deassert a bus grant signal to one of the first bus agent and the second bus agent having a lower grant-to-valid latency in clock cycle n and to deassert a bus grant signal to one of the first bus agent and the second bus agent having a greater grant-to-valid latency in clock cycle n+1, where n is an integer greater than one (1).

17. (Original) The bus arbiter of claim 15, wherein the bus grant signal is one of an address bus grant signal and a data bus grant signal.

18. (Original) The bus arbiter of claim 11, wherein the bus arbiter is an input/output (I/O) controller.

19. (Original) The bus arbiter of claim 11, wherein the bus arbiter is a memory controller.

20. (Original) The bus arbiter of claim 11, wherein the bus arbiter is a system controller.

21. (Original) A system, comprising:

a bus;

at least a first bus agent and a second bus agent coupled to the bus; and

a chipset coupled to the bus including a controller coupled to a bus interface of the chipset, the controller to detect a bus arbitration event between at least the first bus agent and the second bus agent and to grant concurrent bus ownership to the first bus agent and the second bus agent if the first bus agent and a second bus agent have different grant-to-valid latencies.

22. (Currently Amended) The system of claim 21, wherein the controller comprises:

arbitration logic to assert a bus grant signal to both the first bus agent and the second bus agent in a next clock cycle n; and

wherein the arbitration logic is to deassert a bus grant signal to one of the first bus agent and the second bus agent having a lower grant-to-valid latency in clock cycle n+1 and to deassert a bus grant signal to one of the first bus agent and the second bus agent having a greater grant-to-valid latency in clock cycle n+2, where n is an integer greater than one (1).

23. (Original) The system of claim 21, wherein the bus is an on-chip, pipelined shared bus.

24. (Original) The system of claim 21, wherein the chipset comprises a memory controller and an input/output (I/O) controller.

25. (Original) The system of claim 21, wherein the chipset comprises a system controller.

26. (Original) An article comprising a machine readable carrier medium carrying data which, when located into a computer system memory in conjunction with simulation routines, provides functionality of a model comprising:

a controller to detect a bus arbitration event between at least a first bus agent and a second bus agent, the controller to grant concurrent bus ownership to the first bus agent and a second bus agent when the first bus agent and the second bus agent have unequal grant-to-valid latencies.

27. (Currently Amended) The article of claim 26, wherein the controller comprises:

arbitration logic to assert a bus grant signal to both the first bus agent and the second bus agent in a next clock cycle n, where n is an integer greater than one (1); and

wherein the arbitration logic is to deassert a bus grant signal to one of the first bus agent and the second bus agent having a lower grant-to-valid latency in clock cycle n+1 and to deassert a bus grant signal to one of the first bus agent and the second bus agent having a greater grant-to-valid latency in clock cycle n+2.

28. (Original) The article of claim 26, wherein the controller is an input/output (I/O) controller.

29. (Original) The article of claim 26, wherein the controller is a memory controller.

30. (Original) The article of claim 26, wherein the controller is a system controller.